PATENT ABSTRACTS OF JAPAN

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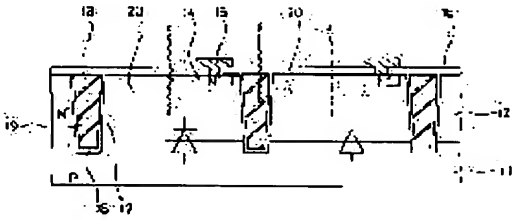
(72)Inventor : TABATA TERUO

(54) OPTICAL SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent a photo diode deteriorated in frequency characteristic due to a parasitic capacitance and adjacent photo diodes from malfunctioning by forming a reverse conductivity type epitaxial layer on a semiconductor substrate and dielectric isolation region piercing the epitaxial layer to the substrate.
SOLUTION: A p-type semiconductor substrate 11 uses a Si single crystal substrate to mechanically support a semiconductor integrated circuit device. An n-type epitaxial layer 12 is laminated on the substrate 11 and dielectric isolation region 13 is composed of trenches 17 extending from the surface of the epitaxial layer 12 to the substrate 11, wall oxide film 18, and dielectric layer 19. This region 13 perfectly surrounds and isolates island regions 20 which form an optical semiconductor device. Thus, the frequency characteristic can be greatly improved to realize a high speed operation. Mutual interference due to flow-in of carriers generated by isolation at the p-n junction is completely avoided and this contributes to the elevation of the degree of integration.



LEGAL STATUS

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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] Optical semiconductor integrated circuit equipment characterized by forming the optical semiconductor device using said epitaxial layer which possessed the dielectric isolation region which penetrated the epitaxial layer and said epitaxial layer of the reverse conductivity type formed on the semi-conductor substrate of one conductivity type, and said semi-conductor substrate, and reached said semi-conductor substrate at least, and was surrounded in said dielectric isolation region.
[Claim 2] Optical semiconductor integrated circuit equipment characterized by forming the optical semiconductor device using said epitaxial layer which possessed the dielectric isolation region which penetrated the epitaxial layer and said epitaxial layer of the reverse conductivity type formed on the semi-conductor substrate of one conductivity type, and said semi-conductor substrate, and reached said semi-conductor substrate at least, and was surrounded in said dielectric isolation region, and the PN junction formed with said semi-conductor substrate.
[Claim 3] Said dielectric isolation region is optical semiconductor integrated circuit equipment according to claim 1 or 2 characterized by being formed with the trench with which even said semi-conductor substrate reached, and the polycrystalline silicon with which said trench was filled up.
[Claim 4] Said optical semiconductor device is optical semiconductor integrated circuit equipment according to claim 1 or 2 characterized by being a photodiode.
[Claim 5] Optical semiconductor integrated circuit equipment characterized by having two or more optical semiconductor devices which used said two or more epitaxial layers which possessed the dielectric isolation region which penetrated the epitaxial layer and said epitaxial layer of the reverse conductivity type formed on the semi-conductor substrate of one conductivity type, and said semi-conductor substrate, and reached said semi-conductor substrate at least, and were surrounded in said dielectric isolation region, and adjoined.
[Claim 6] Said dielectric isolation region is optical semiconductor integrated circuit equipment according to claim 4 characterized by being formed with the trench with which even said semi-conductor substrate reached, and the polycrystalline silicon with which said trench was filled up.
[Claim 7] Said optical semiconductor device is optical semiconductor integrated circuit equipment according to claim 5 characterized by being a photodiode.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the optical semiconductor integrated circuit equipment having optical semiconductor devices, such as a photodiode which used dielectric separation.
[0002]
[Description of the Prior Art] Compared with the integrated circuit device which made each separately and hybridized it, the monolithic light semiconductor integrated circuit equipment which unified the photodiode which is a photo detector, and its circumference circuit can realize a large cost cut, and has the advantage strong also against the noise by electromagnetic field from the exterior.
[0003] That conventional optical semiconductor integrated circuit equipment is indicated to be by JP,1-205564,B is known. Conventional optical semiconductor integrated circuit equipment is explained using drawing 8 and drawing 9 . drawing 8 -- setting -- (1) -- for the bottom isolation region of P+ mold, and (4), as for N+ mold cathode ejection diffusion field and (6), the top isolation region of P+ mold and (5) are [the semi-conductor substrate of P type, and (2) / the epitaxial layer of N-mold, and (3) / a cathode electrode and (7)] silicon oxide.
[0004] With this structure, the PN junction formed between the epitaxial layers (2) surrounded in the semi-conductor substrate (1), the top isolation region (4), and the bottom isolation region (3) is used as a photodiode. In this photodiode, it is detected and used for a cathode ejection diffusion field (5) from the cathode electrode (6) which carried out ohmic contact, using as a current the carrier generated by the light by which incidence is carried out to an epitaxial layer (2).
[0005] Drawing 9 shows the detector. The detection resistance R and Photodiode PD were connected to the serial between DC power supplies E, and the operational amplifier OP has detected the potential of the connection node of Photodiode PD and the detection resistance R. In addition, the capacity C connected to Photodiode PD at juxtaposition is the parasitic capacitance by the depletion layer (8) shown in drawing 8 formed of reverse bias potential between a top and a bottom isolation region (3), (4), and an epitaxial layer (2) by the dotted line.
[0006] Moreover, two adjoining photodiodes are shown by drawing 8 . The detector shown in drawing 9 is connected to each photodiode, respectively, and, naturally it integrates in the same integrated circuit device.
[0007]
[Problem(s) to be Solved by the Invention] However, since the parasitic capacitance by the depletion layer (8) is inevitably formed with the optical semiconductor integrated circuit equipment of this structure, a time constant circuit is formed by the detection resistance R shown in drawing 9 , the frequency characteristics of Photodiode PD worsen, so that parasitic capacitance is large, and it has the trouble which checks high-speed operation.
[0008] Moreover, if incidence of the light is carried out to the isolation region (3) and (4) which have separated between Photodiodes PD when two or more photodiodes PD have been arranged adjacently, as shown in drawing 8 , it will flow to both photodiodes PD with which the carrier

excited by that cause adjoined. Therefore, it had the trouble detected as the incidence of light was made also with the photodiode PD which does not wish for the incidence of light. It also had the trouble of reducing a degree of integration, in response to the constraint which forms in an isolation region (3) big enough and (4) compared with the spot of the light by which incidence is carried out for preventing this, or completely arranges independently photograph DAIO 1 DO PD.

[0009]
[Means for Solving the Problem] This invention was made in view of this conventional technical problem, and offers the optical semiconductor integrated circuit equipment which prevents malfunction of the photodiode with which the frequency characteristics by parasitic capacitance got worse and adjoined by separating the ** PITAKISHARU layer surrounding a photodiode in a dielectric isolation region.
[0010] If it depends on this invention, since the dielectric isolation region is used, there is no generating of the depletion layer by reverse bias potential between a dielectric isolation region and an epitaxial layer, there is no parasitic capacitance by the depletion layer, aggravation of the frequency characteristics of a photodiode can be eliminated, and high-speed operation can be realized. Moreover, since between each photodiode will be separated in the dielectric isolation region when forming two or more adjoining photodiodes if it depends on this invention, even if incidence of the light is carried out to a dielectric isolation region, malfunction between the photodiodes which the carrier excited by the light was not generated but adjoined from the dielectric isolation region can be prevented.
[0011]
[Embodiment of the Invention] This invention is explained below at a detail, referring to a drawing. Drawing 1 is the sectional view showing the optical semiconductor integrated circuit equipment by this invention. Drawing 2 is the top view showing the optical semiconductor integrated circuit equipment by this invention. For the epitaxial layer of N-mold, and (13), as for N+ mold cathode ejection diffusion field and (15), in drawing 1 , a dielectric isolation region and (14) are [(11) / the semi-conductor substrate of P type, and (12) / a cathode electrode and (16)] silicon oxide.
[0012] Since the semi-conductor substrate (11) of P type has the specific resistance of 200 - 1500ohm, and cm and is supporting semiconductor integrated circuit equipment mechanically using a silicon single crystal substrate when semiconductor integrated circuit equipment is completed, it is thickly formed with 300 microns or more. The epitaxial layer (12) of N1 mold grows with the Lynn (P) dope by vapor growth on a semi-conductor substrate (11), and a laminating is carried out to thickness 4-10micro. This thickness is selected by the optimal thickness by the light by which incidence is carried out.
[0013] The dielectric isolation region (13) by which it is characterized [of this invention] consists of dielectric-materials layers (19), such as polycrystalline silicon filled up with about 3000A Wall oxide film (18) which oxidized and formed the trench (17) which even a semi-conductor substrate (11) attains, and its front face from the epitaxial layer (12) front face, and a trench (17). It is the description to surround completely the island field (20) which forms optical semiconductor devices, such as photograph DAIO 1 DO, in this invention in this dielectric isolation region (13). Therefore, as shown in drawing 1 , when forming two or more optical semiconductor devices adjacently, as for both the light semiconductor device, the island field (20) is separated completely in a dielectric isolation region (13).
[0014] The cathode ejection diffusion field (14) of N-mold is formed in the top face of an epitaxial layer (12) of a selection diffusion method at coincidence at the time of the emitter diffusion of an NPN transistor. The cathode electrode (15) of the aluminum which carried out ohmic contact is prepared in the cathode ejection diffusion field (14). Two or more two or more optical semiconductor devices are arranged in seriate, and the optical semiconductor device by this invention mentioned above may be incorporated, as it may be independently incorporated in semiconductor integrated circuit equipment and is shown in drawing 2 . The PN junction in which the epitaxial layer (12) of N-mold with which the semi-conductor substrate (11) of P type formed the common anode field, and this optical semiconductor device was separated separately

in the dielectric isolation region (13) formed the cathode field in, and was formed by the epitaxial layer (12) of a semi-conductor substrate (11) and N-mold constitutes the PN junction of each optical semiconductor device.
[0015] Using the same circuit as what is shown in drawing 9 , the detector of the optical semiconductor device by this this invention prepares a detector according to an individual, when there are two or more optical semiconductor devices. This detector is integrated by the epitaxial layer near the optical semiconductor device (12) although it is natural. In the optical semiconductor device by such this invention, since the epitaxial layer (12) is separated electrically in the dielectric isolation region (13), the seal of approval of the reverse bias potential for separation to a dielectric isolation region (13) becomes unnecessary, and generating of the depletion layer by the reverse bias generated at the time of PN separation becomes that there is nothing. Therefore, there is no generating of the parasitic capacitance by the depletion layer, and the time constant circuit formed by the detection resistance R of the detector shown in drawing 9 can be removed. The frequency characteristics of optical semiconductor devices, such as a photodiode, can be improved sharply by this, and high-speed operation can be realized.

[0016] Moreover, since the spot (21) of the light by which incidence is carried out to the optical semiconductor device according to this individual is usually larger than the width of face of an isolation region when the serial shown in drawing 2 is adjoined and optical semiconductor devices, such as two or more photodiodes, have been arranged, in case it shifts to the optical semiconductor device with which this spot (21) adjoins, ranging over both optical semiconductor devices, incidence is surely carried out. Since the carrier excited by the incidence of this light from the dielectric isolation region (13) is not generated even if incidence of that spot (21) is carried out to this dielectric isolation region (13), since the dielectric isolation region (13) is adopted in this invention, the optical semiconductor device with which incidence of the spot (20) is carried out greatly certainly can be detected, and the mutual intervention by the inflow of the carrier generated in PN-junction separation like before can be prevented completely.
[0017] Then, the manufacture approach of the optical semiconductor integrated circuit equipment by this invention is explained with reference to drawing 7 from drawing 3 below. In drawing 3 , the laminating of the epitaxial layer (12) of N-mold is first carried out on the semi-conductor substrate (11) of P type. At this process, well-known vapor growth carries out the laminating of the epitaxial layer (12) of N-mold of 0.5 ohm-cm extent to about about 4-10micro. The thickness of this shrimp TAKISHARU layer (12) has the thickness which was usually controlled by time amount and was suitable for the light by which incidence is carried out chosen. In addition, an epitaxial layer (12) front face forms the 1st silicon oxide (31) by thermal oxidation.
[0018] In drawing 4 , a trench (17) is formed so that an epitaxial layer (12) may be ****(ed). About 1000A silicon nitride (32) is adhered with a reduced pressure CVD method on the 1st silicon oxide (31). Then, about 5000A phosphorus glass (PSG) layer (33) is adhered with a reduced pressure CVD method on it. After acting as a **-king, in order to carry out selective etching of the 1st silicon oxide (31), silicon nitride (32), and phosphorus glass layer (33) on the trench (17) of a schedule, it covers with a photoresist layer (34) except for the trench (17) top which is a schedule. Then, anisotropy dry etching of the epitaxial layer (12) which removes by anisotropy dry etching in order of a phosphorus glass layer (33), a silicon nitride (32), and the 1st silicon oxide (31), and consists of exposed silicon is performed, and the trench (17) with which even a semi-conductor substrate (11) reaches is formed.
[0019] In drawing 5 , after removing a photoresist layer (34), it is filled up with the polycrystalline silicon layer (36) which is dielectric materials in a trench (17). About 1000A thin dummy oxide film (not shown) is first formed for the side face of a trench (17) by dummy oxidation in 900 degrees C and a steam ambient atmosphere, a phosphorus glass layer (33) is removed further, it oxidizes within 1000 degrees C and a steam ambient atmosphere, and about 3000A Wall oxide film (18) is formed. Next, the polycrystalline silicon of a non dope is adhered to the thickness of about 1.5micro with a reduced pressure CVD method on the whole surface, and the inside of a trench (17) is fill uped with a dielectric-materials layer (19).

[0020] In drawing 6 , ** TCHIBATSUKU of the polycrystalline silicon deposited on the front face is carried out by anisotropic etching, it is removed, and only the polycrystalline silicon in a trench (17) is left behind. Next, using a silicon nitride (32) as a mask, selective oxidation is carried out and about 2500A cap oxide film (35) is formed in the polycrystalline silicon layer (19) top face of a trench (17). Since a silicon nitride (32) is removed after that and a cap oxide film (35) is removed by coincidence, a flat top face is formed.
[0021] In drawing 7 , the cathode ejection diffusion field (14) of N+ mold is formed in the front face of the island field (20) formed by the epitaxial layer (12) surrounded in the dielectric isolation region (13) by the selection diffusion method. For example, a cathode ejection diffusion field (14) is formed in the emitter diffusion and coincidence of an NPN transistor in many cases. After forming a contact hole in the silicon oxide (16) of a cathode ejection diffusion field (14) after that, it adheres in a spatter, dry etching of the aluminum layer is carried out to a predetermined configuration, and a cathode electrode (15) is formed in the whole surface.
[0022] When magnitude is made into one-side the square of L micro for the front face of the epitaxial layer (12) of Photodiode PD and the thickness of an epitaxial layer (12) is assumed to be t micro, the stray capacity Cpn of the photodiode PD in the conventional vertical PN-junction isolation construction shown in Fig. 8 is [0023] expressed with a formula 1.
[Equation 1]

$$Cpn = \frac{\varepsilon_0 \varepsilon_s}{d} S$$

$$= \frac{\varepsilon_0 \varepsilon_s}{d} [L^2 + 4tL]$$

$$Cpn = \frac{\varepsilon_0 \varepsilon_s}{d} [(L+2t)^2 - 4t^2] \quad \cdots \text{式}1$$

[0024] Since d is the width of face (micrometer) of a depletion layer (8) here and it is the function of the applied voltage to PN-junction separation, under the same service condition, it can be regarded as a constant. S is surface area (micrometerxmum) including the side face of Photodiode PD, and can also be expressed with a formula 2.
[0025]
[Equation 2]

$$S = L^2 + 4tL \quad \cdots\cdots \text{式}2$$

[0026] On the other hand, since it is as small as the stray capacity of a side attachment wall can be disregarded, a formula 3 can express stray capacity with the photodiode PD of dielectric separation of this invention.
[0027]
[Equation 3]

$$Ctr = \frac{\varepsilon_0 \varepsilon_s}{d} L^2 \quad \cdots \text{式}3$$

[0028] Therefore, the photodiode of this invention can reduce stray capacity from the photodiode PD of the former [part / of the formula 4 which is the difference of a formula 1 and a formula 3].
[0029]
[Equation 4]

$$\frac{\varepsilon_0 \varepsilon_s}{d} 4tL \quad \cdots \text{式}4$$

[0030] If L is set as 100micro angle and applied voltage to 5micro and PN-junction separation is set to 1V for t, specifically, it will become as in Table 1.
[0031]
[Table 1]

L	従来例	本発明
100μm	42、1fF	35、1fF
50μm	12、3fF	8、8fF

[0032] The property of the stray capacity Cpn of the photodiode PD of the former and this invention is shown in drawing 10 . From drawing 10 , it can decrease about 30% from the stray capacity of the conventional photodiode PD of the same size with the photodiode PD of this invention. Furthermore, if size of Photodiode PD is made small, the ratio (Cpn/Ctr) of the stray capacity of the former and this invention will become large. That is, the ratio of stray capacity can be expressed with a formula 5.

[0033]

[Equation 5]

$$\frac{Cpn}{Ctr} = 1 + \frac{4t}{L} \quad \cdots\cdots \text{式}5$$

[0034] This ratio is shown in drawing 11 . This shows that the PN-junction area of the inferior surface of tongue of Photodiode PD becomes small, and the effectiveness of this invention becomes remarkable further. Therefore, when a small spot condenses like the photodiode for laser beam light-receiving, it becomes the photodiode of an area small naturally, and the reduction effectiveness of the stray capacity by the structure of this invention becomes remarkably large.

[0035] Therefore, in the detector shown in drawing 9 , a cut off frequency fc becomes like a formula 6, and this cut off frequency fc is determined by the stray capacity Ctr of Photodiode PD. The property Fig. which compared the property of a cut off frequency fc with the structure of the former and this invention is shown in drawing 12 .

[0036]

[Equation 6]

$$fc = \frac{1}{2\pi CR} \quad \cdots\cdots \text{式}6$$

[0037] On the other hand, since the sensibility of Photodiode PD is naturally proportional to the area, if it is the same area, it has the sensibility of conventional this invention. However, with the structure of this invention, it becomes possible [high-speed operation] only for the part which can make stray capacity Ctr small. Since a carrier is not excited here even if incidence of the light is carried out to a dielectric isolation region (13) when it adjoins with the structure of this invention and two or more photodiodes PD are finally arranged Even if it is the case where the photodiode by which optical incidence is carried out was located next to [which does not wish for optical incidence] Photodiode PD, and this optical incidence has reached the dielectric isolation region between both (13) The photodiode PD which does not wish for optical incidence can prevent completely the conventional fault of malfunctioning on the carrier excited by the leaver section. Therefore, the array of two or more photodiodes PD is free, and since it is possible to approach further and to arrange from before, it can contribute also to the improvement in a degree of integration.

[0038]

[Effect of the Invention] If it depends on this invention, the frequency characteristics of optical semiconductor devices, such as a photodiode, can be improved sharply, and it has the advantage which can realize high-speed operation as explained above. Moreover, since the mutual intervention by the inflow of the carrier generated in PN-junction separation like before can be completely prevented when two or more photodiodes are arranged adjacently, the array of two or more photodiodes PD is free, and since it is possible to approach further and to arrange from before, it has the advantage which can contribute also to the improvement in a degree of integration.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is a sectional view for explaining the optical semiconductor integrated circuit equipment of this invention.
[Drawing 2] It is a top view for explaining the optical semiconductor integrated circuit equipment of this invention.
[Drawing 3] It is a sectional view for explaining the manufacture approach of the optical semiconductor integrated circuit equipment of this invention.
[Drawing 4] It is a sectional view for explaining the manufacture approach of the optical semiconductor integrated circuit equipment of this invention.
[Drawing 5] It is a sectional view for explaining the manufacture approach of the optical semiconductor integrated circuit equipment of this invention.
[Drawing 6] It is a sectional view for explaining the manufacture approach of the optical semiconductor integrated circuit equipment of this invention.
[Drawing 7] It is a sectional view for explaining the manufacture approach of the optical semiconductor integrated circuit equipment of this invention.
[Drawing 8] It is a sectional view for explaining conventional optical semiconductor integrated circuit equipment.
[Drawing 9] It is a circuit diagram explaining the detector of the optical semiconductor device used for the former and this invention.
[Drawing 10] It is the property Fig. showing the stray capacity Cpn of a photodiode.
[Drawing 11] It is the property Fig. showing the ratio of stray capacity.
[Drawing 12] It is the property Fig. showing a cut off frequency.

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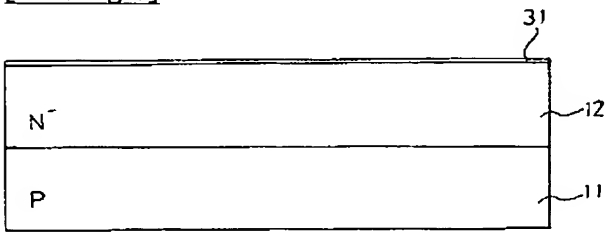
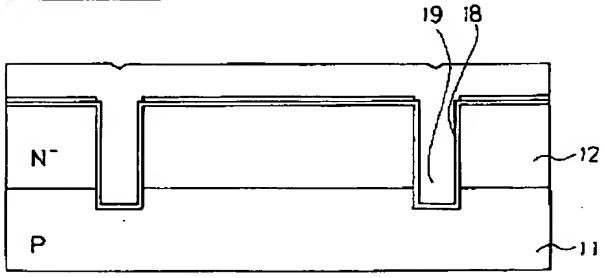
DRAWINGS

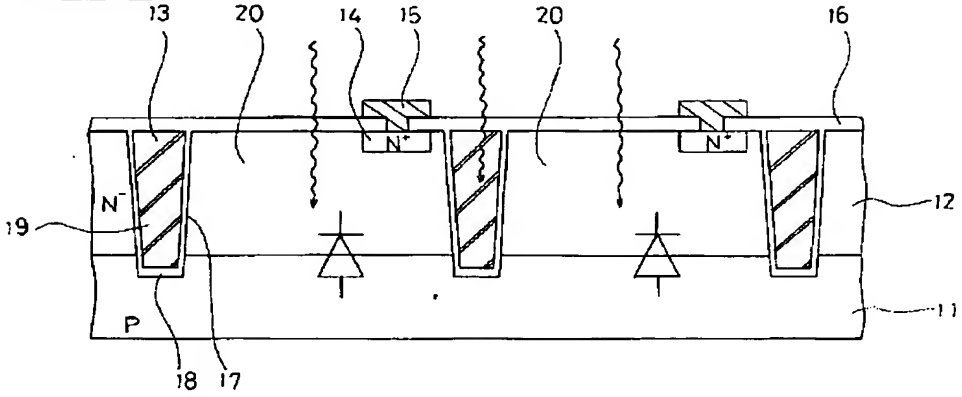
[Drawing 3]



[Drawing 5]

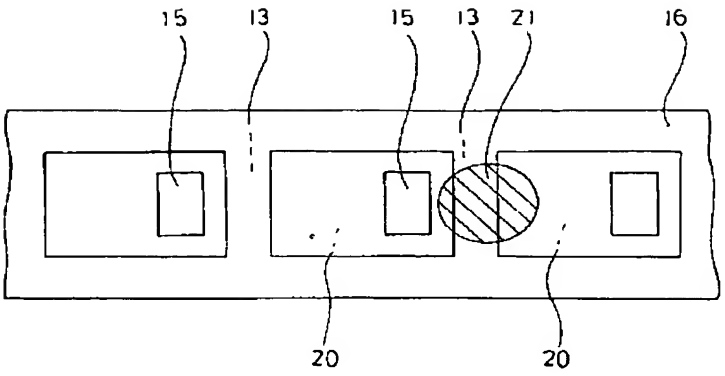


[Drawing 1]

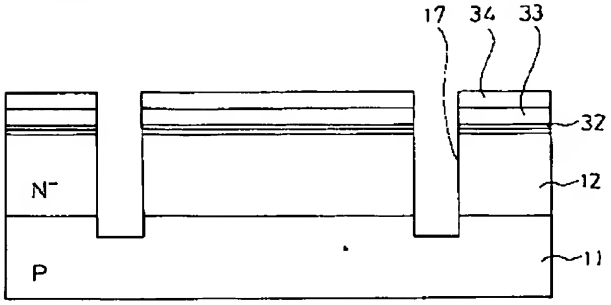


11：基板　12：エピタキシャル層
13：誘電体分離領域　20：島領域

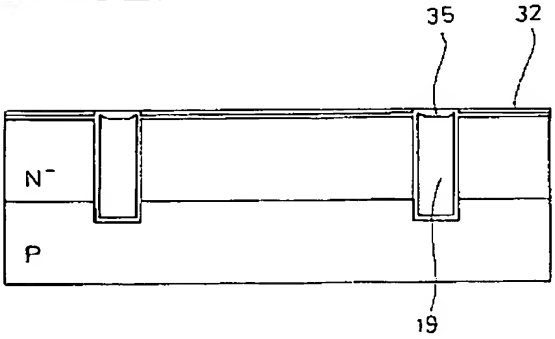
[Drawing 2]



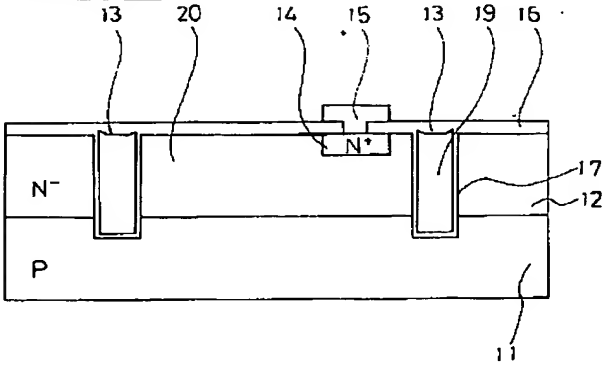
[Drawing 4]



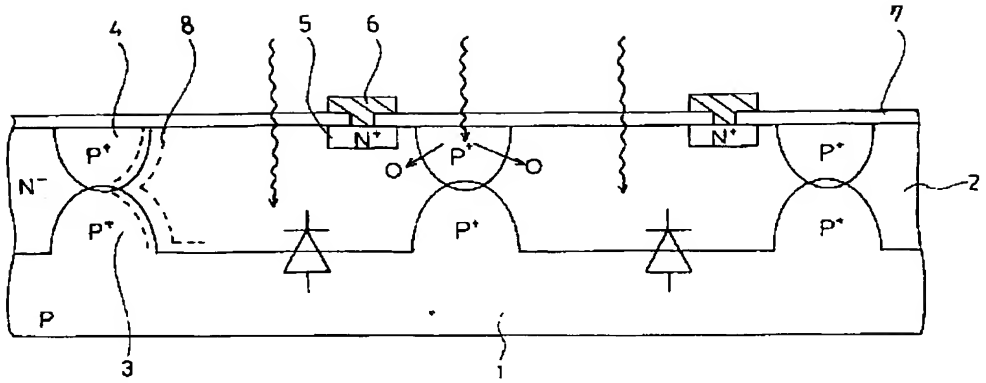
[Drawing 6]



[Drawing 7]

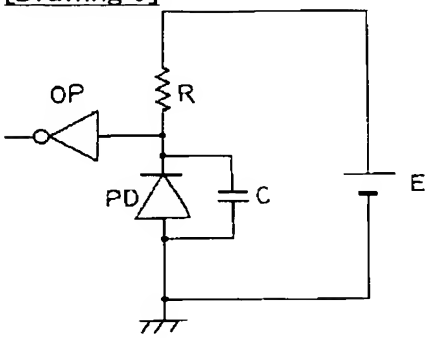


[Drawing 8]

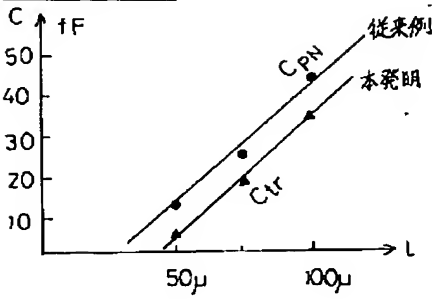


1：P 型半導体基板　　2：N⁻型エピタキシャル層　　3：P⁺型下側分離領域
4：P⁺型上側分離領域　　5：N⁺型カソード取り出し拡散領域
6：カソード電極　　7：酸化膜　　8：空乏層

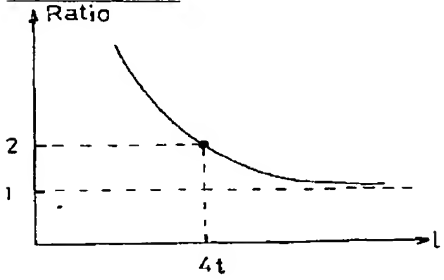
[Drawing 9]



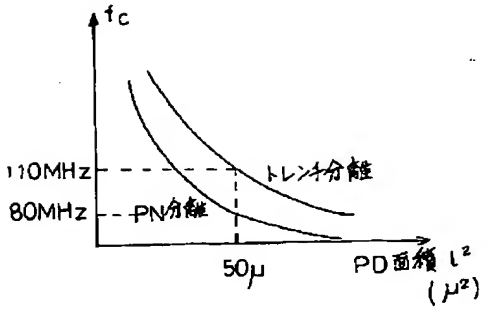
[Drawing 10]



[Drawing 11]



[Drawing 12]



[Translation done.]

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(43)公開日　平成９年(1997)８月15日

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	27/15				27/15	Ｄ	
	31/10				31/10	Ａ	

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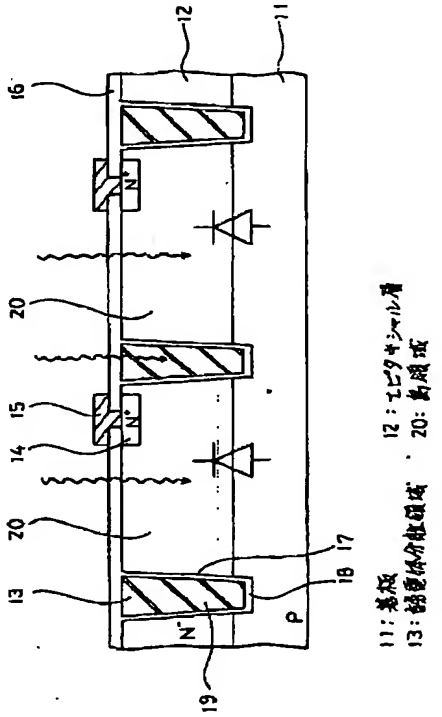
(54)【発明の名称】　光半導体集積回路装置

(57)【要約】
【課題】　エピタキシャル層１２に形成される光半導体装置を分離領域の寄生容量による動作周波数特性の悪化から守る構造を実現し、また複数の光半導体装置間の誤動作から免れる構造を実現する。
【解決手段】　エピタキシャル層１２を半導体基板１１まで到達する誘電体分離領域１３で分離した島領域２０を形成し、この島領域２０にフオトダイオード等の光半導体装置をそれぞれ形成する。また複数の光半導体装置を隣接して形成するときは、個々の光半導体装置を誘電体分離領域１３で囲むように分離する。



【特許請求の範囲】
【請求項１】　一導電型の半導体基板と前記半導体基板上に形成された逆導電型のエピタキシャル層と前記エピタキシャル層を貫通し少なくとも前記半導体基板に到達した誘電体分離領域とを具備し、前記誘電体分離領域で囲まれた前記エピタキシャル層を用いた光半導体装置を形成したことを特徴とする光半導体集積回路装置。
【請求項２】　一導電型の半導体基板と前記半導体基板上に形成された逆導電型のエピタキシャル層と前記エピタキシャル層を貫通し少なくとも前記半導体基板に到達した誘電体分離領域とを具備し、前記誘電体分離領域で囲まれた前記エピタキシャル層と前記半導体基板で形成されたＰＮ接合を用いた光半導体装置を形成したことを特徴とする光半導体集積回路装置。
【請求項３】　前記誘電体分離領域は前記半導体基板まで到達したトレンチと前記トレンチに充填された多結晶シリコンとで形成されたことを特徴とする請求項１または請求項２記載の光半導体集積回路装置。
【請求項４】　前記光半導体装置はフオトダイオードであることを特徴とした請求項１または請求項２記載の光半導体集積回路装置。
【請求項５】　一導電型の半導体基板と前記半導体基板上に形成された逆導電型のエピタキシャル層と前記エピタキシャル層を貫通し少なくとも前記半導体基板に到達した誘電体分離領域とを具備し、前記誘電体分離領域で囲まれ且つ隣接した複数の前記エピタキシャル層を用いた複数の光半導体装置を有することを特徴とする光半導体集積回路装置。
【請求項６】　前記誘電体分離領域は前記半導体基板まで到達したトレンチと前記トレンチに充填された多結晶シリコンとで形成されたことを特徴とする請求項４記載の光半導体集積回路装置。
【請求項７】　前記光半導体装置はフオトダイオードであることを特徴とした請求項５記載の光半導体集積回路装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、誘電体分離を用いたフオトダイオード等の光半導体装置を内蔵する光半導体集積回路装置に関する。
【０００２】
【従来の技術】受光素子であるフオトダイオードとその周辺回路とを一体化したモノリシック光半導体集積回路装置はそれぞれを別個に作りハイブリッド化した集積回路装置に比べて、大幅なコストダウンが実現でき、外部から電磁界による雑音にも強い利点を有している。
【０００３】従来の光半導体集積回路装置は例えば特公平１－２０５５６４号公報に記載されているものが知られている。図８および図９を用いて従来の光半導体集積回路装置について説明する。図８において、（１）はＰ型の半導体基板、（２）はＮ－型のエピタキシャル層、（３）はＰ＋型の下側分離領域、（４）はＰ＋型の上側分離領域、（５）はＮ＋型カソード取り出し拡散領域、（６）はカソード電極、（７）はシリコン酸化膜である。
【０００４】かかる構造では、半導体基板（１）と上側分離領域（４）および下側分離領域（３）で囲まれたエピタキシャル層（２）との間で形成されるＰＮ接合をフオトダイオードとして利用される。このフオトダイオードではエピタキシャル層（２）に入射される光により発生されるキャリアを電流としてカソード取り出し拡散領域（５）にオーミック接触したカソード電極（６）から検出して用いる。
【０００５】図９はその検出回路を示す。直流電源Ｅ間に直列に検出抵抗Ｒとフオトダイオードｐｄを接続し、フオトダイオードｐｄと検出抵抗Ｒの接続ノードの電位をオペアンプＯＰで検出している。なおフオトダイオードｐｄに並列に接続された容量Ｃは上側および下側分離領域（３）（４）とエピタキシャル層（２）間に逆バイアス電位により形成された図８に点線で示した空乏層（８）による寄生容量である。
【０００６】また図８では隣接した２個のフオトダイオードが示されている。それぞれのフオトダイオードには図９に示す検出回路がそれぞれ接続されており、当然同一の集積回路装置内に集積化されている。
【０００７】
【発明が解決しようとする課題】しかしながら、かかる構造の光半導体集積回路装置では空乏層（８）による寄生容量が必然的に形成されるので、図９に示す検出抵抗Ｒとで時定数回路が形成され、寄生容量が大きいほどフオトダイオードｐｄの周波数特性が悪くなり、高速動作を阻害する問題点を有している。
【０００８】また図８に示すように複数のフオトダイオードｐｄを隣接して配置した場合、フオトダイオードｐｄ間を分離している分離領域（３）（４）に光が入射されると、それにより励起されたキャリアが隣接した両方のフオトダイオードｐｄに流れてしまう。そのために光の入射を希望しないフオトダイオードｐｄでも光の入射がなされたと検出される問題点を有していた。これを防止するには入射される光のスポットに比べて充分に大きな分離領域（３）（４）に形成するか、全く独立してフオトダイオードｐｄを配置する制約を受け、集積度を低下させる問題点も有していた。
【０００９】
【課題を解決するための手段】本発明はかかる従来の課題に鑑みなされたもので、フオトダイオードを囲むエピタキシャル層を誘電体分離領域で分離することにより、寄生容量による周波数特性の悪化および隣接したフオトダイオードの誤動作を防止する光半導体集積回路装置を提供するものである。

【００１０】本発明に依れば、誘電体分離領域を用いているので、誘電体分離領域とエピタキシャル層間で逆バイアス電位による空乏層の発生が無く、空乏層による寄生容量が無くフォトダイオードの周波数特性の悪化を排除でき、高速動作を実現できる。また本発明に依れば、隣接した複数のフオトダイオードを形成する場合に各フオトダイオード間を誘電体分離領域で分離しているので、誘電体分離領域に光が入射されても誘電体分離領域からその光により励起されたキャリアは発生されず隣接したフオトダイオード間での誤動作は防止できる。

【００１１】

【発明の実施の形態】以下に本発明を図面を参照しながら詳細に説明する。図１は本発明による光半導体集積回路装置を示す断面図である。図２は本発明による光半導体集積回路装置を示す平面図である。図１において、（１１）はＰ型の半導体基板、（１２）はＮ－型のエピタキシャル層、（１３）は誘電体分離領域、（１４）はＮ＋型カソード取り出し拡散領域、（１５）はカソード電極、（１６）はシリコン酸化膜である。

【００１２】Ｐ型の半導体基板（１１）はシリコン単結晶基板を用い、半導体集積回路装置を完成したときに２００～１５００Ω・ｃｍの比抵抗を有しており、また半導体集積回路装置を機械的に支持しているので３００ミクロン以上と厚く形成されている。Ｎ一型のエピタキシャル層（１２）は半導体基板（１１）上に気相成長法によりリン（Ｐ）ドープで成長され、厚さ４～１０μに積層される。この厚みは入射される光により最適の厚みに選定される。

【００１３】本発明の特徴とする誘電体分離領域（１３）はエピタキシャル層（１２）表面より半導体基板（１１）まで達するトレンチ（１７）とその表面を酸化して形成した約３０００Åのウオール酸化膜（１８）とトレンチ（１７）を充填する多結晶シリコン等の誘電体材料層（１９）とで構成されている。本発明ではフオトダイオード等の光半導体装置を形成する島領域（２０）をこの誘電体分離領域（１３）で完全に取り囲んでいることが特徴である。従って図１に示すように複数の光半導体装置を隣接して形成される場合は両光半導体装置は完全にその島領域（２０）を誘電体分離領域（１３）で分離される。

【００１４】Ｎ－型のカソード取り出し拡散領域（１４）は選択拡散法によりたとえばＮＰＮトランジスタのエミツタ拡散時に同時にエピタキシャル層（１２）の上面に形成される。そのカソード取り出し拡散領域（１４）にはオーミック接触したアルミニウムのカソード電極（１５）を設ける。上述した本発明による光半導体装置は単独で半導体集積回路装置内に組み込まれる場合もあり、また図２に示すように複数の光半導体装置を列状に複数個並べて組み込まれる場合もある。かかる光半導体装置はＰ型の半導体基板（１１）が共通のアノード領域を形成し、誘電体分離領域（１３）で個々に分離されたＮ－型のエピタキシャル層（１２）がカソード領域を形成し、半導体基板（１１）とＮ－型のエピタキシャル層（１２）で形成されたＰＮ接合が各光半導体装置のＰＮ接合を構成している。

【００１５】かかる本発明による光半導体装置の検出回路は図９に示すものと同様の回路を用い、複数個の光半導体装置があるときは個別に検出回路を設ける。当然であるが、この検出回路は光半導体装置の近くのエピタキシャル層（１２）に集積化される。このような本発明による光半導体装置では、エピタキシャル層（１２）を誘電体分離領域（１３）で電気的に分離しているので、誘電体分離領域（１３）に分離のための逆バイアス電位の印可が不要となり、ＰＮ分離のときに発生する逆バイアスによる空乏層の発生が皆無となる。従って空乏層による寄生容量の発生がなく、図９に示す検出回路の検出抵抗Ｒとで形成される時定数回路が除去できる。これによりフオトダイオード等の光半導体装置の周波数特性を大幅に改善でき、高速動作を実現できる。

【００１６】また図２に示す直列に隣接して複数のフオトダイオード等の光半導体装置を配置した場合には、この個別の光半導体装置に入射される光のスポット（２１）が通常分離領域の幅より大きいので、このスポット（２１）が隣接する光半導体装置に移行する際に必ず両方の光半導体装置に跨って入射される。本発明では誘電体分離領域（１３）を採用しているので、そのスポット（２１）がこの誘電体分離領域（１３）に入射されてもこの光の入射により誘電体分離領域（１３）から励起されたキャリアが発生されないので、確実にスポット（２０）が大きく入射されている光半導体装置を検出でき、従来のようなＰＮ接合分離で発生するキャリアの流入による相互干渉を完全に防止できる。

【００１７】続いて以下に本発明による光半導体集積回路装置の製造方法を図３から図７を参照して説明する。まず図３において、Ｐ型の半導体基板（１１）上にＮ－型のエピタキシャル層（１２）を積層する。本工程では周知の気相成長法により０．５Ω・ｃｍ程度のＮ－型のエピタキシャル層（１２）を約４～１０μ程度に積層される。このエピタキシャル層（１２）の厚みは通常時間により制御され、入射される光に適した厚みを選択される。なおエピタキシャル層（１２）表面は第１のシリコン酸化膜（３１）を熱酸化により形成する。

【００１８】図４において、エピタキシャル層（１２）を貫通するようにトレンチ（１７）を形成する。第１のシリコン酸化膜（３１）上に約１０００Åのシリコン窒化膜（３２）を減圧ＣＶＤ法により付着する。続いてその上に約５０００Åのリンガラス（ＰＳＧ）層（３３）を減圧ＣＶＤ法により付着する。ベーキングをした後、予定のトレンチ（１７）上の第１のシリコン酸化膜（３１）、シリコン窒化膜（３２）およびリンガラス層（３

3）を選択エッチングするために予定のトレンチ（17）上を除きフオトレジスト層（34）で被覆する。続いて異方性ドライエッチングによりリンガラス層（33）、シリコン窒化膜（32）、第1のシリコン酸化膜（31）の順に除去し、露出されたシリコンよりなるエピタキシヤル層（12）の異方性ドライエツチングを行い、半導体基板（11）まで到達するトレンチ（17）を形成する。

【0019】図5において、フオトレジスト層（34）を除去した後、トレンチ（17）内に誘電体材料である多結晶シリコン層（36）を充填する。まずトレンチ（17）の側面を900℃、スチーム雰囲気中でダミー酸化により約1000Åの薄いダミー酸化膜（図示せず）を形成し、さらにリンガラス層（33）を除去して1000℃、スチーム雰囲気内で酸化し、約3000Åのウオール酸化膜（18）を形成する。次に、全面にノンドープの多結晶シリコンを約1．5μの厚みに減圧CVD法で付着し、トレンチ（17）内を誘電体材料層（19）で埋める。

【0020】図6において、表面に堆積された多結晶シリコンは異方性エツチングによりエッチバックされて除去され、トレンチ（17）内の多結晶シリコンのみが残される。次にシリコン窒化膜（32）をマスクとして用い、選択酸化してトレンチ（17）の多結晶シリコン層（19）上面に約2500Åのキャップ酸化膜（35）を形成する。その後シリコン窒化膜（32）を除去し、同時にキャップ酸化膜（35）も除去されるので平坦な上面が形成される。

【0021】図7において、誘電体分離領域（13）で囲まれたエピタキシヤル層（12）で形成された島領域（20）の表面には選択拡散法によりN＋型のカソード取り出し拡散領域（14）を形成する。たとえば、カソード取り出し拡散領域（14）はNPNトランジスタのエミッタ拡散と同時に形成される場合が多い。その後カソード取り出し拡散領域（14）のシリコン酸化膜（16）にコンタクト孔を形成した後、全面にアルミニウム層をスパッターで付着し、所定形状にドライエッチングしてカソード電極（15）を形成する。

【0022】フォトダイオードPDのエピタキシャル層（12）の表面を大きさを1辺Lμの正方形とし、エピタキシャル層（12）の厚みをtμと仮定すると、第8図に示す従来の上下PN接合分離構造におけるフォトダイオードPDの浮遊容量Cpnは式1で表される

【0023】

【数1】

$$Cpn = \frac{\varepsilon_0 \varepsilon_s}{d} S$$

$$= \frac{\varepsilon_0 \varepsilon_s}{d} [L^2 + 4tL]$$

$$Cpn = \frac{\varepsilon_0 \varepsilon_s}{d} [(L+2t)^2 - 4t^2] \quad \cdots \text{式1}$$

【0024】ここでdは空乏層（8）の幅（μm）であり、PN接合分離への印加電圧の関数であるので、同一の使用条件下では定数とみなせる。Sはフォトダイオードの側面を含めた表面積（μm×μm）であり、式2で表すこともできる。

【0025】

【数2】

$$S = L^2 + 4tL \quad \cdots\cdots \text{式2}$$

【0026】一方本発明の誘電体分離のフォトダイオードPDでは、側壁の浮遊容量は無視できる位小さいので、式3で浮遊容量を表すことができる。

【0027】

【数3】

$$Ctr = \frac{\varepsilon_0 \varepsilon_s}{d} L^2 \quad \cdots \text{式3}$$

【0028】従って、式1と式3との差である式4の分だけ、従来のフォトダイオードPDより本発明のフォトダイオードの方が浮遊容量を低減できる。

【0029】

【数4】

$$\frac{\varepsilon_0 \varepsilon_s}{d} 4tL \quad \cdots \text{式4}$$

【0030】具体的には、Lを100μ角、tを5μ、PN接合分離への印加電圧を1Vとすると表1の通りとなる。

【0031】

【表1】

L	従来例	本発明
100μm	42、1fF	35、1fF
50μm	12、3fF	8、8fF

【００３２】図１０に従来と本発明のフォトダイオードＰＤの浮遊容量Ｃｐｎの特性を示す。図１０から、本発明のフォトダイオードＰＤでは同一サイズの従来のフォトダイオードＰＤの浮遊容量より約３０％も減少できる。更にフォトダイオードＰＤのサイズを小さくすると、従来と本発明の浮遊容量の比（Ｃｐｎ／Ｃｔｒ）は大きくなる。即ち、浮遊容量の比を式５で表すことができる。

【００３３】

【数５】

$$\frac{Cpn}{Ctr} = 1 + \frac{4t}{L} \quad \cdots\cdots \text{式５}$$

【００３４】このレシオを図１１に示す。これはフォトダイオードＰＤの下面のＰＮ接合面積が小さくなり、更に本発明の効果が顕著になることを示している。従ってレーザ光受光用のフォトダイオードのように小さいスポットに凝縮される場合は当然小さい面積のフォトダイオードとなり、本発明の構造による浮遊容量の削減効果は著しく大きくなる。

【００３５】従って図９に示す検出回路では、カットオフ周波数ｆｃは式６のようになり、フォトダイオードＰＤの浮遊容量Ｃｔｒによりこのカットオフ周波数ｆｃは決定される。カットオフ周波数ｆｃの特性を従来と本発明の構造とで比較した特性図を図１２に示す。

【００３６】

【数６】

$$fc = \frac{1}{2\pi CR} \quad \cdots\cdots \text{式６}$$

【００３７】一方、フォトダイオードＰＤの感度は当然その面積に比例するので、同一面積であれば従来の本発明の感度を持つ。しかし本発明の構造では浮遊容量Ｃｔｒを小さくできる分だけ高速動作が可能となる。最後に、本発明の構造では隣接して複数のフォトダイオードＰＤを配列した際に、誘電体分離領域（１３）に光が入射されてもここではキャリアが励起されないので、光入射を希望しないフォトダイオードＰＤの隣に光入射されているフォトダイオードが位置し、該光入射が両者間の誘電体分離領域（１３）にも及んでいる場合であっても、光入射を希望しないフォトダイオードＰＤが分離部分で励起したキャリアで誤動作するといった従来の欠点を完全に防止できる。従って複数のフォトダイオードＰＤの配列が自由であり、また従来より更に近接して配置することが可能であるので、集積度向上にも寄与できる。

【００３８】

【発明の効果】以上に説明したとおり、本発明に依ればフォトダイオード等の光半導体装置の周波数特性を大幅に改善でき、高速動作を実現できる利点を有する。また、隣接して複数のフォトダイオードを配列した場合は、従来のようなＰＮ接合分離で発生するキャリアの流入による相互干渉を完全に防止できるので、複数のフォトダイオードＰＤの配列が自由であり、また従来より更に近接して配置することが可能であるので、集積度向上にも寄与できる利点を有するものである。

【図面の簡単な説明】

【図１】本発明の光半導体集積回路装置を説明するための断面図である。

【図２】本発明の光半導体集積回路装置を説明するための平面図である。

【図３】本発明の光半導体集積回路装置の製造方法を説明するための断面図である。

【図４】本発明の光半導体集積回路装置の製造方法を説明するための断面図である。

【図５】本発明の光半導体集積回路装置の製造方法を説明するための断面図である。

【図６】本発明の光半導体集積回路装置の製造方法を説明するための断面図である。

【図７】本発明の光半導体集積回路装置の製造方法を説明するための断面図である。

【図８】従来の光半導体集積回路装置を説明するための断面図である。

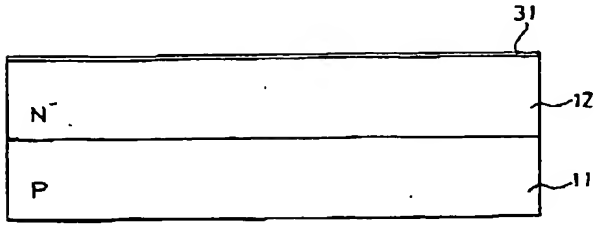
【図９】従来および本発明に用いる光半導体装置の検出回路を説明する回路図である。

【図１０】フォトダイオードの浮遊容量Ｃｐｎを示す特性図である。

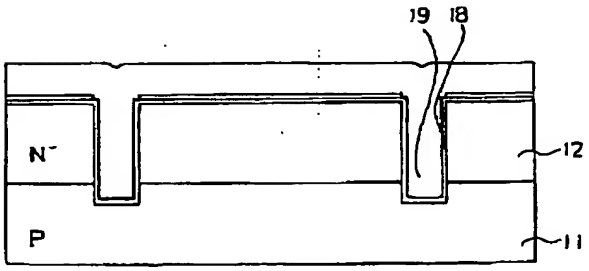
【図１１】浮遊容量の比を示す特性図である。

【図１２】カットオフ周波数を示す特性図である。

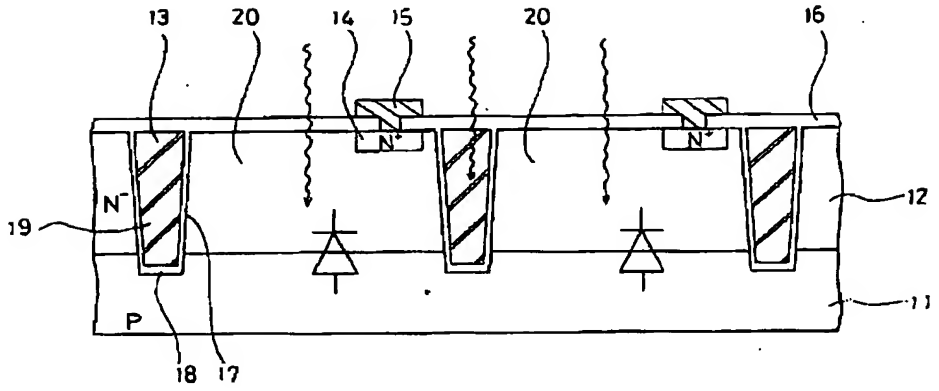
【図３】



【図５】

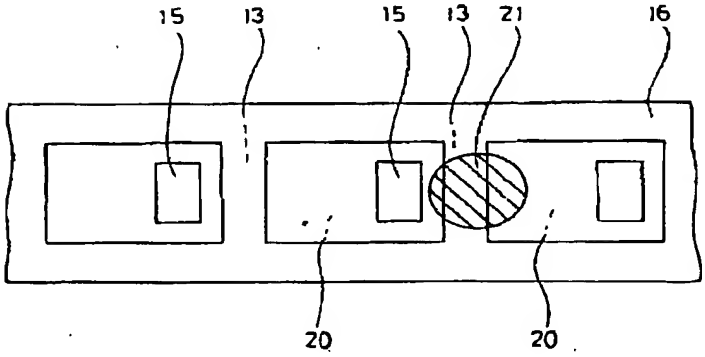


【図1】

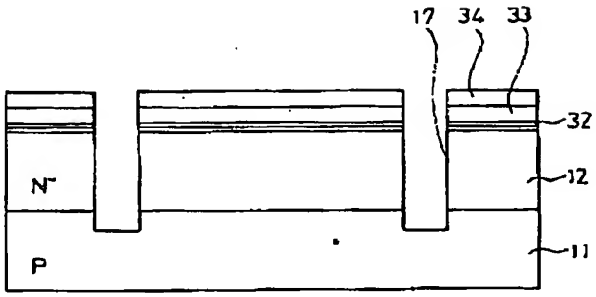


11：基板　12：エピタキシャル層
13：絶縁体分離領域　20：島領域

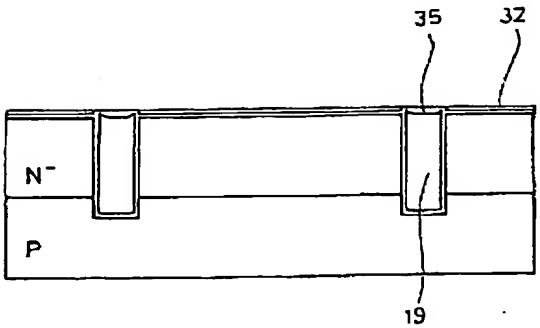
【図2】



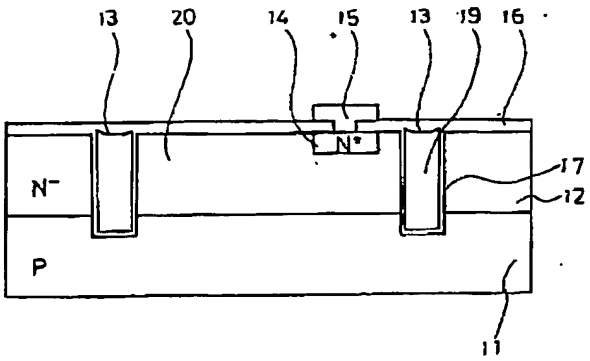
【図4】



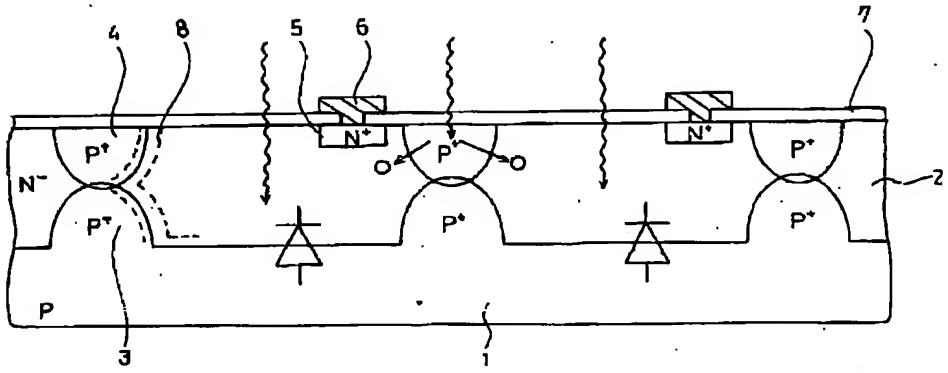
【図6】



【図7】

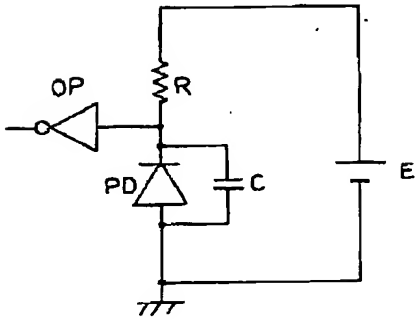


【図８】

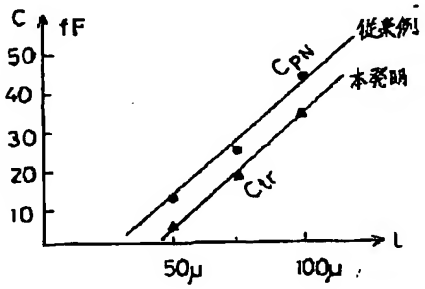


1：P 型半導体基板　2：N⁻型エピタキシャル層　3：P⁺型下側分離領域
4：P⁺型上側分離領域　5：N⁺型カソード取り出し拡散領域
6：カソード電極　7：酸化膜　8：空乏層

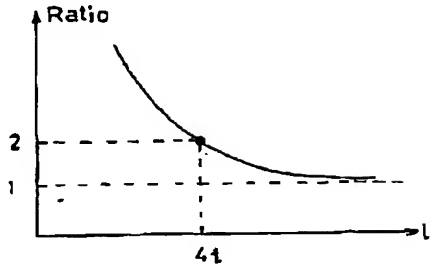
【図９】



【図１０】



【図１１】



【図１２】